Practical determination of individual element resistive states in selectorless RRAM arrays

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***Abstract*—Three distinct methods of reading multi-level cross-point resistive states from selector-less RRAM arrays are implemented in a physical system and compared for read-out accuracy. They are: the standard, direct measurement method and two methods that attempt to enhance accuracy by computing cross-point resistance on the basis of multiple measurements. Results indicate that the standard method performs as well as or better than its competitors. SPICE simulations are then performed with controlled amounts of non-idealities introduced in the system in order to test whether any technique offers particular resilience against typical practical imperfections such as crossbar line resistance. We conclude that even though certain non-idealities are shown to be minimised by different circuit-level read-out strategies, line resistance within the crossbar remains an outstanding challenge.**

***Index Terms* - Crossbar, RRAM, SPICE, measurement technique, analogue circuits, memory, device characterisation**

I. Introduction

Resistive Random-Access Memory (RRAM) is a promising, emerging, beyond-Moore memory technology whereby storage nodes operate on the basis of the resistive switching phenomenon. RRAM systems exhibit small size and good scalability (down to $8 \times 8\,nm$ node size reported in the literature) [1], [2], multi-state memory storage [3], low-power operation [4] and rely on the use of simple, 2-terminal devices; all highly desirable characteristics for applications ranging from large, industrial memory cells to neuromorphic applications. In neuromorphic engineering RRAM is seen as a possible means of linking pre- and post-synaptic neurons through area-effective artificial synapses [5]; currently a fundamental stumbling block towards the development of large-scale, area- and power-efficient artificial brain-inspired computational systems.

The key benefit of RRAM scalability is typically leveraged by implementing RRAM cells as crossbar arrays; a configuration that maximises memory area density (down to $4F^2$/storage node for planar crossbars, where F is the minimum feature size of the crossbar array [6], [7]). The main drawback of this implementation, however, is the issue of 'sneak currents' [8] whereby current tends to pass through devices other than the device under test (DUT) during 'read' and 'write' operations (Fig. 1). Sneak currents prove disruptive to the accuracy of read operations [9] and may precipitate programming of non-target storage nodes during write operations.

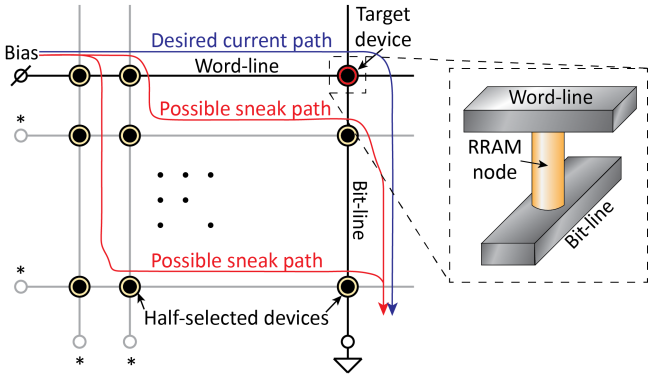

Fig. 1. The crossbar sneak current problem: when attempting to interface a target device 'sneak current' will flow through 'sneak paths', thus corrupting the accuracy of read operations and potentially disrupting non-target devices during the write operation. The specific paths and magnitudes of sneak currents will depend on the biasing regime applied to the nodes marked as '*'. Inset shows the structure of each cross-point.

Research towards mitigating sneak current effects revolves mainly around the development of 'selector devices' that can be embedded into the storage nodes themselves and allow highly selective targeting of DUTs [10]–[12]. The implementation of selector devices, however, adds complexity to the overall fabrication process. Sneak currents can be mitigated in selectorless arrays too by e.g. employing suitable biasing regimes (for overview of such biasing regimes see section 2.6 in [13]) or attempting to calculate cross-point resistance via multiple, multi-port measurements [14]. Each mitigation/read-out strategy has merits and drawbacks.

In this paper we build upon previous work [15] and investigate the readout accuracy limits in selectorless, multi-level RRAM crossbar arrays for three distinct read-out techniques. We implement them on a custom-built instrumentation platform and compare their ability to successfully read resistive states from a small (12×12), selectorless reference array consisting of linear resistors. We then further broaden the scope of our study by extrapolating towards the scaling limits of RRAM selectorless arrays as well as worst-case scenarios via SPICE simulations. The focus is kept on well-behaved linear test devices in order to eliminate any sources of uncertainty that would be present if RRAM devices had been used (inadvertent switching, resistive state drift etc.).

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The capability of performing accurate array-level read-outs is a crucial element in many applications. One example is the mass testing of novel device architectures, where array-level electrical characterisation would be a major boost towards the automation of the process development cycle. Another example can be found in multi-level memory cell development, where the amount of information potentially extractable from storage nodes able to assume resistive states within a continuous range is read-out accuracy-limited. Finally, the field of neuromorphic engineering could exploit the benefits arising from the development of nanoelectronic artificial synapse banks far more efficiently if there was an option to monitor the internal state of every synapse in the bank for debugging and analysis purposes.

The paper is organised as follows: Section II provides the definition of 'memory state' and introduces the three different read-out techniques. Section III presents a physical system capable of performing all three types of read operation whilst section IV provides measured results from our prototyped reference array used to assess the instrument's accuracy. Section V presents SPICE simulations whereby system performance is estimated for larger arrays set up in standard 'worst-case' configurations. Finally, section VI discusses the merits of each read operation technique in light of the simulated and measured results and draws the overall conclusions of the paper.

II. Theoretical Background

A. Defining a memory state

The resistive state (RS) of any two-terminal, non-linear component (such as typical RRAM devices) can be measured in a multitude of ways, e.g. as the static or differential resistance as measured when some fixed potential difference (ΔV) is applied across the component. In practice it is convenient to use the static resistance at fixed ΔV definition. This approach is amenable to easy circuit implementation as it employs a constant read-out voltage and allows for the determination of DUT RS via a simple amperometric measurement. In this work, we define RS as static resistance measured at $\Delta V = 0.5\,V$. This value was arbitrarily chosen in order to demonstrate sub-volt operation whilst allowing our instrumentation platform to operate well above the noise floor. Read-out voltage optimisation lies outside the scope of this paper.

B. Crossbar array nomenclature

Reading from a crossbar array typically involves targeting a single cross-point element at a time and attempting to determine its resistive state. This gives rise to 'active' (leading to the target device) and 'inactive' word- and bit-lines. In order to simplify the tangled structure of the crossbar network, read-out operations are typically performed with all inactive word-lines shorted together and similarly all inactive bit-lines shorted together. This reduces the crossbar network to a 'four-node-four-component' (4n4c) system where the four components are: 1) the target device alone (R_T), 2) the devices sharing word-line with the target (we shall call this the 'word complement' of R_T) with equivalent resistance R_w, 3) the devices sharing bit-line with the target (the 'bit complement' of R_T) with equivalent resistance R_b and 4) the rest of the array with equivalent resistance R_r (see [9], [14]). Fig. 2 illustrates these concepts. We shall use this reduced system in order to describe how the three read-out operations function conceptually.

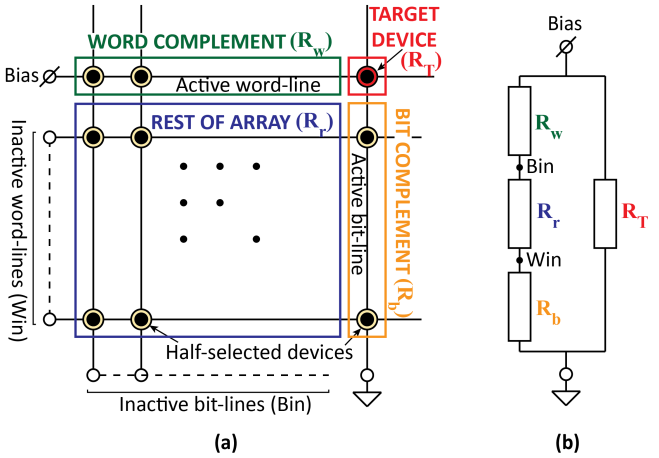

Fig. 2. Crossbar array terminology: (a) Once a device has been selected for a read or write operation the array is split into four sub-arrays and the word- and bit-lines are classified as active or inactive depending on whether they lead to the target device or not. (b) '4n4c' approximation of array when inactive word- and bit-lines are shorted together.

C. The three read-out techniques

1) Single read - one direct measurement: There are many biasing regimes that can be used to carry out a 'single read' operation. The specific choice of regime will depend largely on the type of device being used (e.g. unipolar- vs. bipolar-switched) and other considerations, such as power dissipation, but ultimately it will aim to simultaneously determine the voltage drop across, and the current through the target device:

$$R_T = \frac{V_b}{i_T} \tag{1}$$

where R_T is the target resistance to be determined, V_b denotes the standard read-out voltage applied across the target device (in this work $V_b = 0.5\,V$) and i_T is the current through the target device. i_T can be determined by bootstrapping the word- or bit-complement devices (or both) and measuring current entering/exiting the active line servicing the bootstrapped devices. An example of a possible single read measurement configuration is shown in Fig. 3(a). A good way to implement it in practice would be by realising the ammeter as a trans-resistance amplifier (TRA), thus enforcing virtual earthing of the active bit-line. This, in turn, ensures bootstrapping of the bit-complement whilst keeping the voltage drop across the target device under control as shown in Fig. 3(b).

This technique is relatively easy to implement and relies on a single measurement, but when the target device is in very high RS, i_T becomes very small. This generates vulnerability to systematic offset error factors such as constant leakage currents and especially voltage offsets that affect the quality

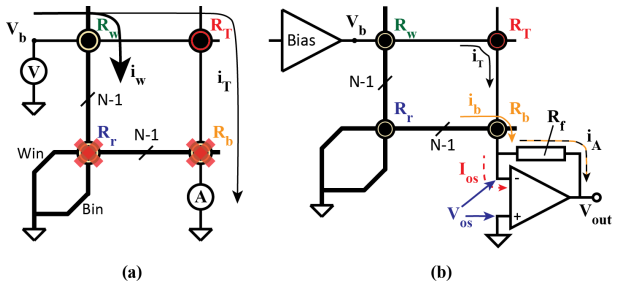

Fig. 3. Example of a 'single read' operation: (a) Ideal concept where the voltage source provides a known bias, whilst the ammeter measures the current through the target device i_T. A significant amount of current may pass through the word-complement (i_w) towards GND. R_b is bootstrapped in this example while R_r is shunted. (b) Possible circuit implementation where a trans-resistance amplifier (TRA) plays the role of the ammeter. Amplifier offset voltage (V_{os}) and current (I_{os}) are shown explicitly.

of bootstrapping as seen in Fig. 3(b). The importance of proper bootstrapping for the correct operation of the single read technique can be demonstrated by calculating the current reaching the ammeter in the example of figure 3(b) if amplifier offset voltage $V_{os} \neq 0$ and offset current I_{os} small:

$$i_A = i_T + i_b = \frac{V_b - V_{os}}{R_T} - \frac{V_{os}}{R_b(V_{os})} \approx \frac{V_b}{R_T} - \frac{V_{os}}{R_b(V_{os})} \quad (2)$$

where i_A is the current through the ammeter, i_b the current through the $(N-1)$ devices constituting R_b, $R_b(V_{os})$ the static resistance of the R_b component at a bias voltage of V_{os} and $V_{os} \ll V_b$ in the approximated r.h.s. If V_{os} is small, then the magnitudes of i_T and i_b become comparable when $\frac{V_b}{V_{os}} = \frac{R_T}{R_b}$, which can impose severe constraints on the choice of V_b if R_b is significantly lower than R_T. This would be the case when R_T is in high RS and $R_b(V_{os})$ low.

2) Differential read - two direct measurements: The differential read technique consists of two sub-operations: a standard single read operation under bias voltage $V_{b,1} = V_b = 0.5\,V$ and an additional single read operation performed under zero bias voltage $V_{b,2} = 0\,V$. Computed target resistance for a differential read operation is given by:

$$R_T = \frac{V_{b,1} - V_{b,2}}{i_{t,1} - i_{t,2}} = \frac{V_b}{i_{t,1} - i_{t,2}} \quad (3)$$

where $i_{t,1}$, $i_{t,2}$ is the current through R_T during the first and second sub-operations respectively. $i_{t,2}$ will compensate $i_{t,1}$ for systematic offsets present in the system.

The differential read technique computes static resistance at $V_b = 0.5\,V$ independent of the shape of the target device I-V characteristic only for $V_{b,2} = 0\,V$. Any other choice of $V_{b,2}$ causes the technique to yield the $\Delta V/\Delta I$ slope defined by the two chosen voltage bias points along the I-V of the target device. If we set $V_{b,1} \approx V_{b,2}$, the differential technique attempts to compute differential resistance at the chosen bias point $\frac{\partial V}{\partial I}(V_b)$.

The main benefit of a 'differential read' approach is its offset cancelling nature, which becomes apparent only when systematic offsets become significant sources of error, overpowering sources of random error such as instrumentation

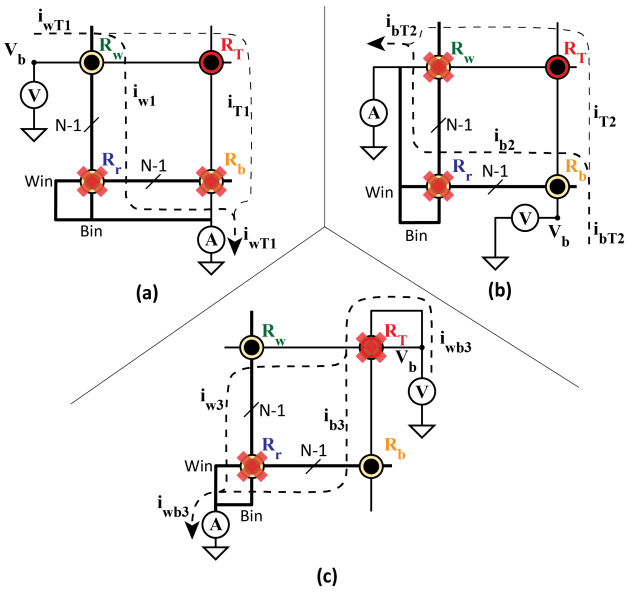

Fig. 4. Conceptual example of triple read operation: (a) Step 1: determine $R_w||R_T$. (b) Step 2: determine $R_b||R_T$. (c) Step 3: determine $R_w||R_b$. The entire cross-bar is considered as a two-terminal black box throughout the operation. The very low resistance component R_r is always shunted for power consumption reasons.

noise. However, the technique requires two sub-operations, one of which is a single read operation; therefore, it is slower than the single read technique.

3) Triple read - three proxy measurements: The 'triple read' operation is based upon the idea of computing R_T by proxy. The procedure flows as follows (see Fig. 4): a) Measure the equivalent resistance of all devices in the target word-line (the 'full word' with equivalent resistance $R_{wT} = R_w||R_T$). b) Measure the resistance of the target bit-line ('full bit', $R_{bT} = R_b||R_T$). c) Short together and bias the active word- and bit-lines with the aim of shunting R_T whilst determining the 'full complement', $R_{wb} = R_w||R_b$. The procedure yields three equations for three unknowns and hence R_T can be computed, as shown in [14]. All read-outs are performed at the standard $V_b = 0.5\,V$.

The equations for each sub-operation are as follows:

$$R_{wT} = \frac{V_b}{i_{wT,1}} \quad (4)$$

$$R_{bT} = \frac{V_b}{i_{bT,2}} \quad (5)$$

$$R_{wb} = \frac{V_b}{i_{wb,3}} \quad (6)$$

where $i_{x,y}$ indicates current through R_x during the yth sub-operation.

It then follows that:

$$G_T = \frac{G_{wT} + G_{bT} - G_{wb}}{2} \Rightarrow R_T = \frac{2V_b}{i_{wT,1} + i_{bT,2} - i_{wb,3}} \quad (7)$$

where $G_x = \frac{1}{R_x}$.

Although algebraically a correct method for determining R_T, this method suffers from an inherent tendency to amplify errors committed while determining its partial results R_{bT}, R_{wT} and R_{wb}. Let us define the fractional read-out error of any single read measurement F as:

$$F = \frac{R_{meas} - R_{nom}}{R_{nom}} \tag{8}$$

where R_{nom} is the nominal and R_{meas} the measured RS of the target element(s). Noting that $G_{xy} = G_x + G_y$ it can be show that computed target device conductance $G_{T,meas}$ in the presence of read-out errors is given by:

$$\begin{aligned} 2 \cdot G_{T,meas} = (1+\alpha)(G_w + G_T) + (1+\beta)(G_b + G_T) \\ - (1+\gamma)(G_w + G_b) \end{aligned} \tag{9}$$

where α, β, γ are the fractional errors in reading G_{wT}, G_{bT} and G_{wb} respectively and G_T the actual target device conductance.

The fractional error in determining G_T is then given by:

$$\frac{G_{T,meas} - G_T}{G_T} = \frac{\alpha+\beta}{2} + \frac{(\alpha-\gamma)G_w}{2 \cdot G_T} + \frac{(\beta-\gamma)G_b}{2 \cdot G_T} \tag{10}$$

Eq. 10 shows that the fractional error involved in reading G_{wT} and G_{bT} transmits directly into the fractional error in reading G_T, but the terms $(\alpha-\gamma)$ and $(\beta-\gamma)$ are amplified by $\frac{G_w}{G_T}$ and $\frac{G_b}{G_T}$ respectively. Furthermore, the Bienayme formula[1] and the variance scaling property[2] tell us that any variance in α, β and γ (random read-out errors e.g. due to noise in the circuitry) will be amplified by $\frac{G_w}{G_T}/\frac{G_b}{G_T}$ and add-up to cause higher final computed R_T variance vs. variance in measurements of R_{wT}, R_{bT} and R_{wb}.

Theoretically, the main benefit of using this technique would be that the entire crossbar array is treated as a two-terminal device in every sub-operation. This implies that unlike in single and differential read-out, all current entering the array will exit through the ammeter, whilst the exclusive use of shunting (as opposed to bootstrapping) in order to neutralise various components of the crossbar (e.g. R_b or R_w) should remove the requirement for careful handling of offsets. However, this technique requires three sub-operations to complete and the ability of the system to treat each crossbar line as either a word- or a bit-line flexibly. The relatively minor increase in circuit complexity needed to accommodate this additional flexibility is overshadowed by the fact that during the last sub-operation current flows through both R_w and R_b, but in opposite polarities from the perspective of the DUTs. Therefore, this read-out technique is not suitable for arrays consisting of storage nodes with asymmetric I-V curves.

As a side-note we notice a further benefit of this technique concerning speed: Each sub-operation aims to compute a low resistance formed by the parallel combination of either N or $(2N-1)$ devices. Consequently, for sufficiently large 'N' the determination of all l.h.s. terms in equations 4, 5 and 6 can potentially be much faster than obtaining a 'single' or 'differential' read result. This speed benefit will tend to improve with increased array size. The detailed study of the transient behaviour of the three read-out techniques is outside the scope of this paper where we concentrate on steady-state behaviour (read-outs are assumed to be taken when all voltages throughout the system have settled).

[1]The variance of the sum or difference of n uncorrelated random variables equals the sum of their n individual variances.

[2]The variance of $k \cdot X$, where X is a random variable and k a constant, equals k times the variance of X.

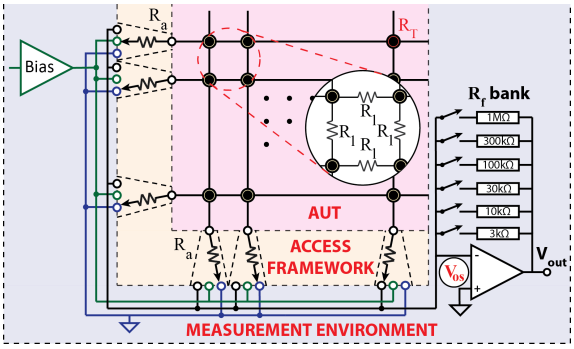

Fig. 5. Simplified instrumentation platform schematic showing the 'Array Under Test' (AUT, pink), the access framework (yellow) and the measurement environment (blue). Key sources of error are also shown: access resistance R_a, line resistance R_l and TRA offset voltage V_{os}.

III. System Implementation

Fig. 5 shows a simplified schematic of the instrumentation platform used to implement the read-out techniques under study. At the core sits the crossbar array under study. Around it lies the access framework module, which consists of single-pole-triple-throw (SP3T) switches whose positions determine which lines act as active and inactive word- and bit-lines. Pairs of relays (G6EU-134P-US) were used in order to implement the SP3T functionality whilst minimising access resistance (R_a - $50m\Omega$ max.). Finally, the measurement environment consists mainly of the bias generator and the TRA. The TRA consists of a precision OpAmp (OPA227 - $\pm 200\,\mu V$ max. offset) and its feedback resistor (R_f) bank (precision resistors - 5/6 resistors at 0.1% tol. 1/6 at 1%) and acts as an ammeter with output voltage V_{out} as its current-reading variable. The R_f bank allows the TRA to measure a large range of currents whilst maintaining V_{out} within the amplifier's output swing limits. Each resistor in the R_f bank is software-assigned to measure target loads within given RS ranges (table I). The boundaries between the RS ranges of adjacent R_f resistors are given by their geometric means. The bias generator consists of an LT1970A amplifier whose output is measured each time a device is read in order to improve measurement accuracy.

At higher level the system is operated by a microcontroller (mBED LPC1768) and implemented on a custom-made PCB with discrete components. This is crucial as it allowed us to utilise very high spec components in order to test the limits of read-out accuracy. Other system modules, not shown in the schematic of Fig. 5, include: read-out buffers, voltage references, the power management unit and the device programming unit. A photograph of the instrument is shown in Fig. 6.

TABLE I
TARGET LOAD RS CLASSES.

Class ID	R_f ($k\Omega$)	Min. RS ($k\Omega$)	Max. RS ($k\Omega$)	n^*
1	3	0	5.48	28
2	10	5.48	17.3	50
3	30	17.3	54.7	39
4	100	54.7	173	25
5	300	173	547	2
6	1000	547	∞	0

* Number of devices in reference crossbar (see section IV).

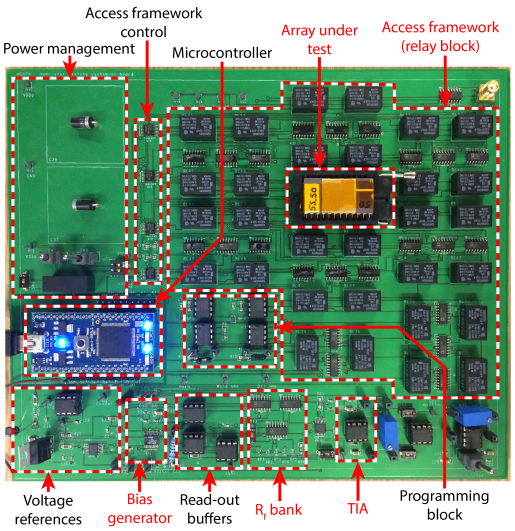

Fig. 6. Photograph of PCB-based instrumentation platform implementing the read-out techniques under study. Blocks referred to in Fig. 5 are labelled in red.

IV. EXPERIMENTAL RESULTS

The performance of the 'single', 'differential' and 'triple' read-out techniques was benchmarked against a reference crossbar array. The array consisted of discrete, linear resistors with RS ranging between $1\,k\Omega$ and $220\,k\Omega$ (Fig. 7); values covering the initially intended region of operation of the instrument ($1\,k\Omega - 100\,k\Omega$). Notable features of the reference array include: a) An all-low RS ($1\,k\Omega$) bit-line intended to uncover the effects of attempting to bootstrap a very low RS path. b) A high RS ($> 100\,k\Omega$) word-line testing read-out performance at excessively high RS. c) Components randomly drawn from pots of available devices to provide insight concerning read-out of intermediate-value components in a relatively homogeneous environment.

Every device in the reference crossbar was measured with each technique described in section II and the fractional read-out error was computed. Results obtained from measurements on the reference array are shown in Fig. 8. Notably, results for the single and differential read-out techniques are very similar and cover broadly similar ranges in terms of F. On the other hand, results obtained for the triple read show fractional errors up to thousands of percentage points above and below nominal. This is rather surprising considering that the partial results for full word, full bit and full complement are all fairly tightly distributed.

Panels (d) and (e) in figure 8 show characteristic horizontal,

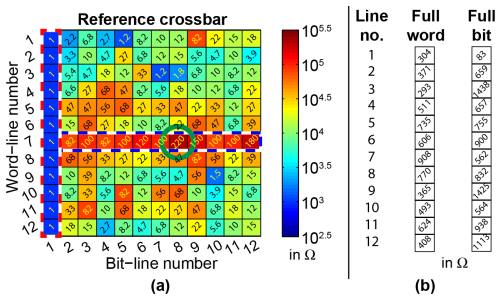

Fig. 7. Reference resistor crossbar array used for assessing read-out quality: (a) Resistor configuration. Numbers at each cross-point location indicate RS in $k\Omega$. White/red dashed line: all-low RS bit-line. White/blue dashed line: high RS word-line. Green-circled device: $220\,k\Omega$ RS; the highest value in the reference array. Numbers in each cell indicate device resistance in $k\Omega$. (b) Full word and full bit resistances. Numbers in each box are in Ω.

respectively vertical bands. This is because the triple read sub-operations used to determine the full word or full bit RS are procedurally identical and therefore results should not depend on the specific selection of target device. As a result, panels (d) and (e) of Fig. 8 contain 12 independent measurements of each full word and full bit RS; one for each device in a line. Differences within each set of 12 measurements reveal the effects of random measurement errors. These effects are summarised in table II where for each word/bit line, average fractional error $\overline{F}$ over all 12 measurements and corresponding standard deviation (σ) were computed. σ can be a useful indicator of spread in the data even though the underlying distribution may not necessarily be Gaussian.

TABLE II
AVERAGE FULL WORD AND FULL BIT MEASUREMENT FRACTIONAL ERROR $\overline{F}$ AND STANDARD DEVIATION σ BY WORD-/BIT-LINE IN %.

	Full word		Full bit	
Line number	$\overline{F}$	σ	$\overline{F}$	σ
1	2.506	0.188	3.571	0.117
2	2.718	0.168	4.483	0.223
3	2.392	0.117	6.292	0.229
4	3.428	0.318	3.799	0.218
5	3.927	0.269	3.752	0.149
6	3.559	0.219	4.033	0.143
7	3.798	0.299	3.354	0.194
8	3.756	0.167	4.202	0.213
9	2.191	0.189	6.263	0.394
10	3.071	0.253	3.023	0.224
11	3.490	0.232	4.017	0.294
12	2.714	0.214	4.524	0.266
Average	**3.129**	**0.219**	**4.276**	**0.222**

Many pairs of lines are read with statistically significant fractional error differences ($\Delta\overline{F}$ significantly larger than both associated standard deviations σ) as can be seen by examining e.g. the cells highlighted in yellow in table II (two-tailed two-means t-test shows values of $\overline{F}$ are significantly different with p-value ≈ 0.00095). This indicates that each line is read at a fundamentally distinct fractional error; possibly a function of the RS of the line itself and/or the state of the rest of the crossbar array. This is important because it implies that the fractional errors committed in measuring the terms in the l.h.s. of eq. 7 do not necessarily cancel each other out. At a higher level we also observe that our reference array's word- and

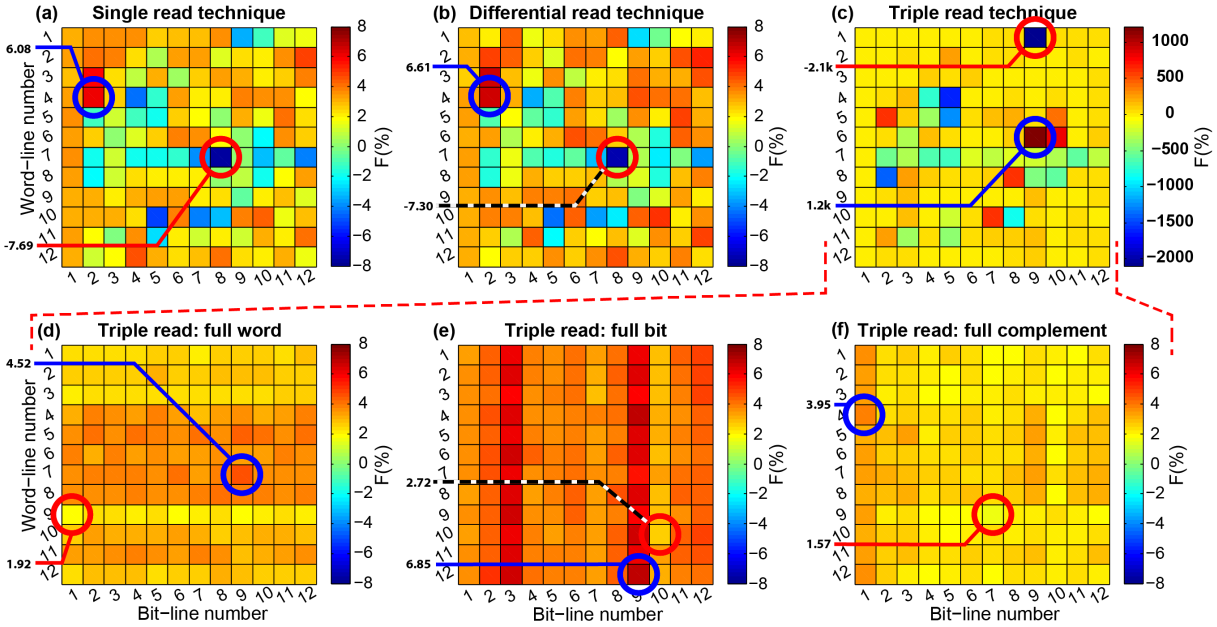

Fig. 8. Fractional read-out errors F obtained by reading the reference crossbar array: (a-c) Results for single, differential and triple read-out techniiques. (d-f) Partial results that combine through eq. (7) to yield panel (c). Devices showing maximum and minimum errors are circled in blue or red circles respectively. Note that all panels except (c) have been plotted vs. the same colour-bar range.

bit-lines are read at significantly different average fractional errors although for both each line contains readings with, on average, similar spread.

Revisiting eq. 10 we note that the $\frac{G_w}{G_T}$ and $\frac{G_b}{G_T}$ factors take large values for some devices, as evidenced in Fig. 7: for example the device sitting at (word, bit) location (7,8) has a value of $220\,k\Omega$ whilst its corresponding full word and full bit have values of $908\,\Omega$ and $832\,\Omega$ respectively. If we set device (7,8) as the target, then we obtain $\frac{G_w}{G_T} = \frac{R_T}{R_w} \approx 242.3$ and $\frac{R_T}{R_b} \approx 264.4$. Even in the absence of systematic fractional errors $\overline{F} = 0$, this would lead relatively small amounts of random error in determining α, β and γ (see σ values in table II) to generate intolerably high read-out errors on most trials.

In order to investigate the resulting data further, the distributions of fractional errors and their corresponding cumulative distributions were extracted for each read-out technique as shown in Fig. 9, top two rows. The bottom row shows cumulative error distributions separately for devices belonging to each RS class. Notably, both single and differential read-out show a propensity for overestimating smaller resistances whilst underestimating larger ones. In both cases the worst performers tend to be the devices in RS class 5. The relatively large number of devices in RS classes 1 and 2 skews the overall error distribution towards a $\approx 3\%$ average overestimate. In the triple read case, the error distribution shows a vast range of values, including many resistances that were read as negative ($F < -100\%$ implies $R_{meas} < 0$). Devices exhibiting higher RS tend to suffer much higher read-out errors.

V. SPICE ANALYSIS

In order to investigate how the three read-out techniques can be expected to perform in the presence of a controlled amount of realistic non-idealities, each was examined through SPICE simulations based on the simplified system schematic in fig. 5. Table III shows the list of non-ideality factors taken into account, of which R_l, R_a and V_{os} were of key significance. All non-ideality factors except R_l were based on the components used in our system and kept fixed for all simulations. The TRA core amplifier was modelled behaviourally, although result accuracy was validated with the more computationally demanding SPICE model provided by the supplier of the component (Texas Instruments).

TABLE III
VALUES OF MEASUREMENT INSTRUMENT AND CROSSBAR ARRAY NON-IDEALITY FACTORS USED IN SIMULATIONS SHOWN IN THIS WORK.

Parameter	Symbol	Value	Units
Line resistance	R_l	50†- 10600‡	$m\Omega$
Access resistance	R_a	300*	$m\Omega$
TRA offset voltage	V_{os}	-10§	μV
TRA output impedance	R_{TRA}	100§	$\mu\Omega$
TRA open loop DC gain	AOL	10^8§	-

† Conservative theoretical calculation for strip-board line resistance.
‡ Theoretical calculation for $100 \times 10\,nm$ cross-section Pt electrode in a $100\,nm$ pitch crossbar.
* G6EU-134P-US relay datasheet and multimeter readings.
§ OPA227 datasheet typ. value.

The simulated system was first tested with the reference array from fig. 7 in order to compare performance against the physical system and then with a 12×12 'worst-case' array with $R_{ON} = 1\,k\Omega$ and $R_{OFF} = 100\,k\Omega$. R_l was $50\,m\Omega$ in both cases. We define 'worst-case' arrays as $N \times N$ arrays consisting of linear I-V elements where the device farthest from the access resistors, in our case devices with (word,bit) coordinates of (1,N), is at the maximum allowed RS (R_{OFF}) whilst every other cross-point node is set at the minimum RS

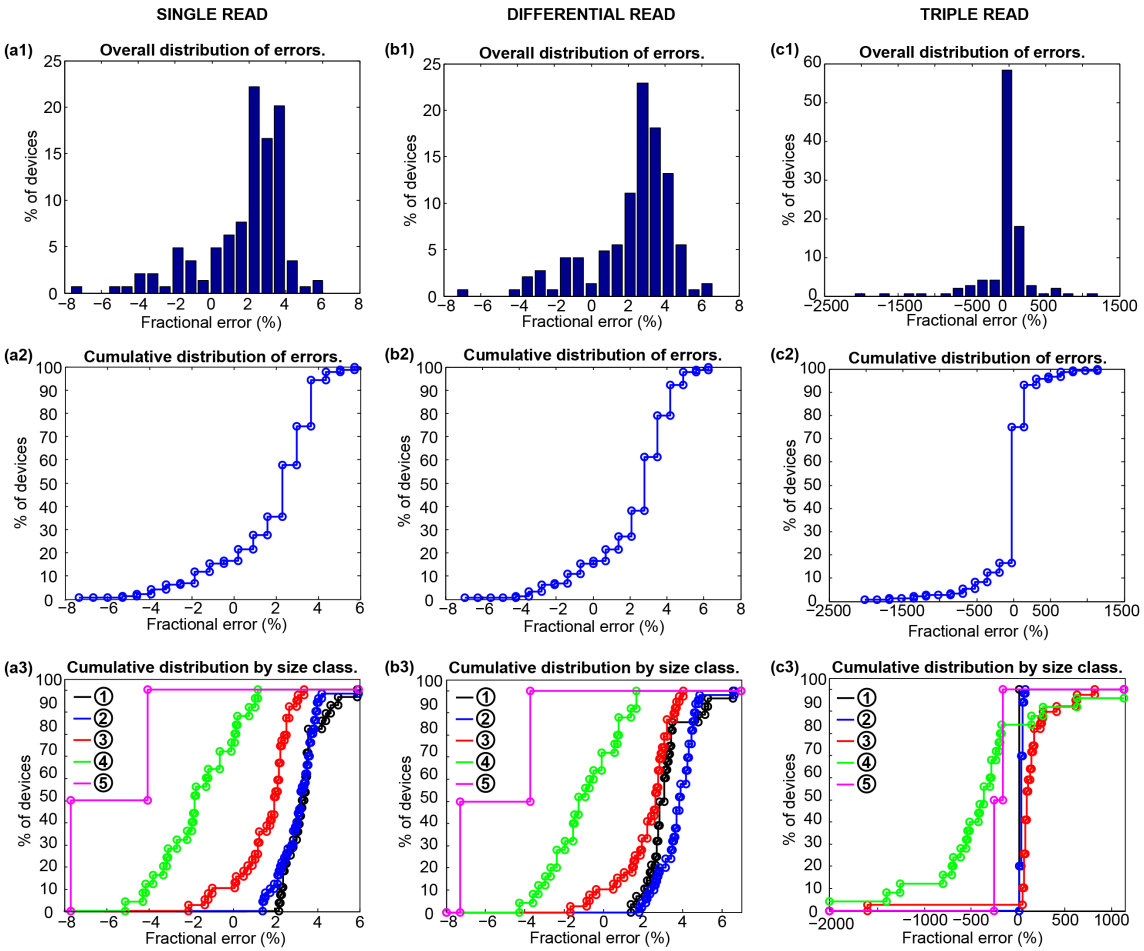

Fig. 9. Fractional read-out error distributions for measurements obtained employing (a) single, (b) differential and (c) triple read-out techniques. Absolute distributions (top row), cumulative distributions (middle row) and cumulative distributions by RS class (bottom row) are shown. Circled numbers in the bottom row map plot colours to RS class.

(R_{OFF}) -see fig. 10(d)-. Results are summarised in fig. 10.

Results on the reference array show that under the simulated system set-up the low RS bit-line exhibits significantly higher errors than the rest of the array due to the effects of line resistance. This is confirmed by noting that as one moves closer towards the bit-line access switch (towards word-line 12) the errors abate in a gradual fashion. This issue affects all read-out techniques similarly. Next, we notice that only in the case of the single read we can still observe traces of the pattern present in fig. 8(a). This pattern vanishes when the single read operation is simulated with an offset-free TRA. The differential and triple read techniques seem to eliminate much of the propensity of the single read technique to underestimate devices at high RS, likely because of the offset-cancelling nature of the differential read.

Results on the 12×12 worst-case array confirm that the differential and triple reads mitigate high RS device underestimation, as seen in the table inset in fig. 10(d). In the case of the triple read the R_{OFF} device is read successfully because word- and bit-complements are read with exactly the same $F \approx 0.5881\%$ whilst the full complement is read at an extremely close $F \approx 0.5880\%$. The main contribution to the final overall read-out F of 0.73% comes from the first r.h.s term of eq. (10) ($\approx 0.59\%$).

Interestingly, in this particular array set-up it is the worst of the R_{ON} devices that forms the bottleneck of the design. Worst R_{ON} shows a fairly consistent $F \approx +1.35\%$ and is located at address (2,11) for all read-out techniques (marked in a red box in fig. 10(d)). Notably, this is the device farthest from the word- and bit-line access switches that does not have an R_{OFF} device on either of its lines; results underlining that the worst performing device is not always the most obvious one (typically assumed to be the high RS device).

Next, simulations were carried out in a variety of worst-case arrays of different sizes and R_l. R_l was swept between a minimum of $50\,m\Omega$ corresponding to expected line resistance for the reference array and a maximum of $10.6\,\Omega$, corresponding to expected line resistance for an array employing Pt electrodes with $100 \times 10\,nm$ cross-sectional area and $100\,nm$ pitch. The fractional read-out errors for the high RS device are shown in figure 11.

Read-out accuracy is very similar for all read-out techniques indicating that line resistance and overall system loading affect all three read-out techniques similarly in the idealised simulation framework used in this section. We notice three key trends. First, small arrays with low line resistance tend to

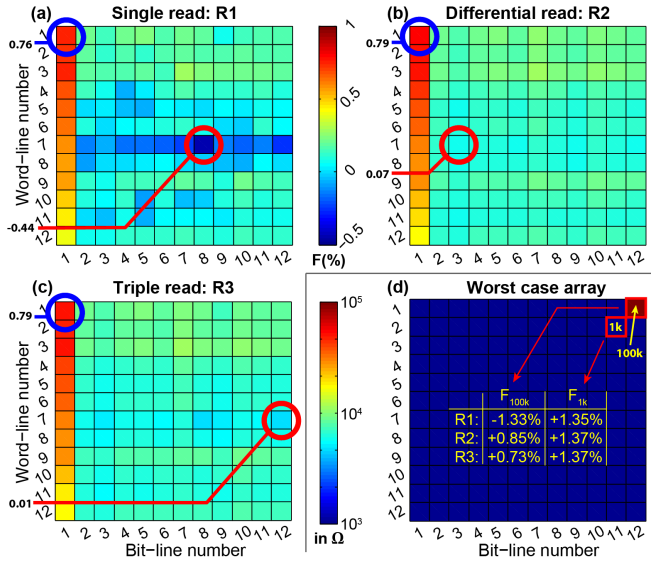

Fig. 10. Performance of simulated crossbar array read-out system (see table III): (a-c) reference crossbar array from fig. 7. Fractional read-out errors F for each read-out technique are shown with devices exhibiting maximum and minimum F marked with blue, respectively red circles; upper colour-bar. (d) Typical 'worst-case' array where all devices are at $R_{ON} = 1\,k\Omega$ except the device farthest from the word- and bit-line access switches, which is set at $R_{OFF} = 100\,k\Omega$; lower colour-bar. Tabulated data inside the array shows F for the R_{OFF} device and the worst of the R_{ON} devices. The R_{ON} device showing the largest F magnitude was found to be the same for all read-out techniques and is marked in a red box.

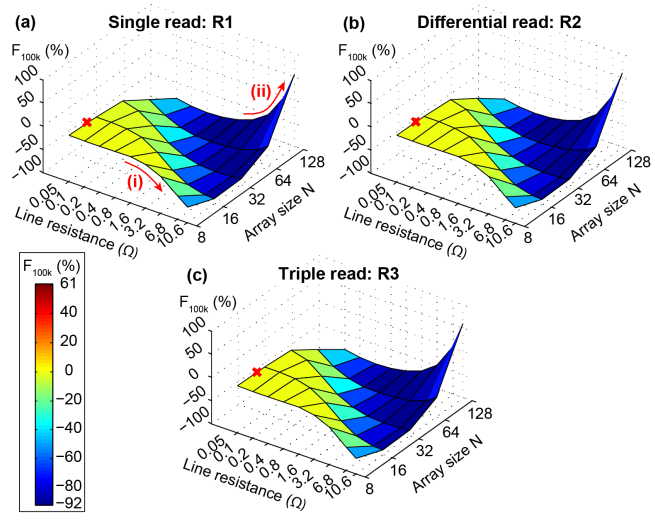

Fig. 11. SPICE-simulated fractional read-out errors of high RS device (F_{100k}) in 'worst-case'-configured arrays for: (a) single read, (b) differential read and (c) triple read techniques as a function of array size (N) and line resistance (R_l). The small red crosses indicate the points in the (N, R_l) space for which the values in the inset table of fig. 10(d) were taken. All panels share colour-bar; in panel (a) interesting trends are marked as (i) and (ii) -see text-.

allow for accurate read-out of the target device, as expected, but as line resistance increases target resistance starts to be underestimated (fig. 11(a) marked (i)). This is probably caused by the line resistance interfering with the bootstrapping/shunting of the active line(s). For example in fig. 3 the inactive word-lines can no longer be assumed to be sufficiently well grounded throughout their entire lengths, thus resulting in above ground voltages at the word-line terminals of the bit-complement devices. When the inactive bit-line terminals of the bit-complement devices are below those of their word-line terminals (a situation aided by low i_T currents) extra current is injected onto the active bit-line and hence the TRA block overestimates the current through the target element. Secondly, if line resistance continues to grow the system tends to start overestimating target element resistance (fig. 11(a) marked (ii)). This probably occurs because voltage delivery to the target element fails completely, all current between bias generator and grounding effectively by-passing the target element and choosing shorter pathways throughout the array. Finally, we notice that for larger arrays the two aforementioned trends continue to be present, but manifest their presence at lower values of R_l.

VI. Discussion

In this paper we have examined the issue of accurate read-out of the resistive state of devices within linear, selectorless crossbar arrays. We have presented three read-out techniques, analysed some of their key sources of errors, implemented a system capable of carrying them all out, presented measured data from a reference array and performed simulations in order to better understand the unique attributes of each technique.

Our analysis indicates that the differential read technique becomes advantageous vis-a-vis the more traditional single read if systematic offsets within the system are a significant source of error. In the noiseless, simplified simulated system we see a clear accuracy benefit although in the physical system it seems that other sources of error dominate - errors that cannot be eliminated through use of the differential read technique.

With regard to the triple read technique, we showed that it has an in-built tendency to amplify differences in the read-out errors of its partial results. Interestingly, in the simulated system these 'partial errors' tended to cancel each other out, which shows that the triple read technique exhibits some degree of inherent resilience to the controlled imperfections we introduced in our simulated system. In the physical system they failed to cancel out and led to extraordinarily high RS read-out errors, possibly because of the highly randomised and asymmetric configuration of the reference array used as a test subject. Finally, we noted that the triple read technique requires employing at least two different read-out voltages throughout its cycle (in our case standard V_{read} and $-V_{read}$). This renders it hard to operate on practical devices with asymmetric I-V curves.

Finally, we have shown simulated results indicating that none of the examined read-out techniques can truly compensate for the inherent limitations arising from within the array

(line resistance, selectorless nature) much more successfully than the others; even when many other sources of error are factored out. This, in combination with the fact that the region of satisfactory operation in (R_l, N)-space is rather restricted points towards the absolute necessity of operating crossbar arrays with high quality selectors.

This work can be pursued further by attacking three crucial issues: a) Introducing transient analysis in order to fully investigate issues of read-out speed and power dissipation, b) measuring and simulating arrays with non-linear, possibly asymmetric IV cross-point elements and c) assessing system performance on arrays that boast selector devices, ideally 2-terminal selectors integrated into the array fabric.

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